This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A method of exchanging data within a direct memory access arrangement including a plurality of IP blocks, the method comprising the steps of:

associating with said IP blocks respective DMA modules each including an input buffer and an output buffer;

coupling said respective DMA modules over a data transfer facility in a chain arrangement where each DMA module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain;

causing each of said DMA modules to interact with the respective IP block by writing data from the input buffer of the DMA module into the respective IP block and reading data from the respective IP block into the output buffer of the DMA module; and

operating said input and output buffers in such a way that:

said writing of data from the input buffer of the DMA module into the respective IP block is started when the respective input buffer is at least partly filled with data; ~~,~~ and

when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain or, in the case of the last DMA module in the chain, are provided as output data;

associating with said output buffers and input buffers coupled in the chain at least one intermediate block to control data transfer between said coupled buffers; and

controlling transfer of data between said coupled buffers over said data transfer facility by issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of:

data existing to be transferred and enough space existing for receiving said data when transferred;

issuing at least one corresponding acknowledgment towards said requesting buffer confirming that the said at least one transfer condition is met; and

transferring data between said requesting buffer and said coupled buffer, whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement.

2. (canceled).

3. (previously presented) The method of either of claims 1 or 2, further comprising the steps of:

including a CPU in said arrangement;

using said CPU for transferring data to be processed into the input buffer of the first DMA module in said chain; and

using said CPU for collecting said output data from the output buffer of the last DMA module in said chain.

4. (previously presented) The method of claim 3, further comprising the step of

configuring said DMA modules via said CPU.

5. (currently amended) ~~Architecture of a direct memory access module for exchanging data between a plurality of IP blocks, the architecture~~An apparatus, comprising:

a ~~data transfer facility~~bus;

a processor coupled to the bus; and

a plurality of respective direct memory access (DMA) modules each associated with ~~said~~ a different IP ~~blocks~~block, the DMA modules being coupled ~~over said data transfer facility~~to each other over the bus, each DMA module including:

an input buffer ~~arranged for writing~~configured to write data into a respective one of the IP ~~block~~ blocks and ~~exchanging~~ exchange data with said ~~data transfer facility~~bus, and

an output buffer ~~arranged for reading~~configured to read data from said respective IP block and ~~exchanging~~ exchange data with said ~~data transfer facility~~bus, said DMA modules being ~~arranged~~ coupled together by the bus in a chain so that each of said DMA modules, other

than the last in the chain, has its respective output buffer coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its input buffer coupled to the output buffer of another of said DMA modules upstream in the chain.

6. (currently amended) The ~~architecture~~ apparatus of claim 5 wherein at least one of said input and output buffers has a fixed data width with respect to said data transfers facility and a selectively variable data width with respect to said respective IP blocks.

7. (currently amended) The ~~architecture~~ apparatus of claim 5 or 6, further comprising

a slave interface module configured ~~for reading~~to read from outside the ~~architecture~~ apparatus data relating to at least one parameter selected from the group consisting of:

a parameter indicating how many bits are available for reading in at least one of said input ~~buffer~~buffers,

a parameter indicating how many bits are present in at least one of said input ~~buffer~~buffers,

a parameter indicating how many bits are available for reading in at least one of said output ~~buffer~~buffers, and

a parameter indicating how many bits are present in at least one of said output ~~buffer~~buffers.

8. (currently amended) The ~~architecture~~ apparatus of claim 5 further comprising

a reprogrammable finite state machine ~~arranged for driving~~configured to drive operation of said ~~architecture~~ apparatus by ~~taking~~ receiving data from at least one of said input ~~buffer~~buffers, downloading data into said respective IP block corresponding to said at least one of said input buffers, receiving data from said respective IP block, and storing data in at least one of said output ~~buffer~~buffers.

9. (currently amended) The ~~architecture~~ apparatus of claim 5 wherein at least one of said input buffers and output buffers is associated with a respective master block ~~for exchanging~~that is

configured to exchange data between the associated buffer and said ~~data transfer facility~~bus, said master block being ~~adapted~~ configured to be coupled in a data exchange relationship to a buffer in a homologous direct memory access module in an arrangement, wherein said master block and said buffer coupled thereto are configured ~~for~~to:

~~issuing~~ issue at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of data existing to be transferred and enough space existing for receiving said data when transferred;

~~issuing~~ issue at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met; and

~~transferring~~ transfer data between said requesting buffer and said coupled buffer, whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement.

10. (canceled)

11. (new) An apparatus, comprising:

a bus;

a processor coupled to the bus; and

a plurality of respective direct memory access (DMA) modules each associated with a different circuit block, the DMA modules being coupled to each other over the bus, each DMA module including:

a first buffer configured to write data into a respective one of the circuit blocks and exchange data with said bus, and

a second buffer configured to read data from said respective circuit block and exchange data with said bus, said DMA modules being coupled together by the bus in a chain so that each of a plural subset of the DMA modules has its respective second buffer coupled to the first buffer of another of said plurality of DMA modules and each of said plural subset of DMA modules has its respective first buffer coupled to the second buffer of another of said DMA modules.

12. (new) The apparatus of claim 11, wherein the plurality of DMA modules comprises three DMA modules.

13. (new) The apparatus of claim 11, wherein at least one of said first and second buffers has a fixed data width with respect to said bus and a selectively variable data width with respect to said respective circuit blocks.

14. (new) The apparatus of claim 11, wherein each of said circuit blocks comprises an IP block.

15. (new) The apparatus of claim 11, wherein said processor comprises a central processing unit (CPU).